CLAIMS

1. A method for determining overlay tolerance for a lot of semiconductor wafers comprising:

measuring a first patterned layer on some of said semiconductor wafers so as to obtain a first set of critical dimension error measurements;

measuring a second patterned layer on some of semiconductor wafers so as to obtain a second set of critical dimension error measurements; and

determining overlay tolerance for said lot of semiconductor wafers using said first set of critical dimension error measurements, said second set of critical dimension error measurements and a line edge placement specification for said lot of semiconductor wafers.

2. The method of Claim 1 wherein said measuring a first patterned layer further comprises:

selecting from said lot of semiconductor wafers a first set of sample wafers; and

measuring critical dimension error at a plurality of locations on each semiconductor wafer in said first set of sample wafers.

3. The method of Claim 2 wherein said measuring a second patterned layer further comprises:

selecting from said lot of semiconductor wafers a second set of sample wafers; and

measuring critical dimension error at a plurality of locations on each semiconductor wafer in said second set of sample wafers.

4. The method of Claim 1 wherein said determining overlay tolerance for said lot of semiconductor wafers further comprises:

determining overlay tolerance for said lot of semiconductor wafers using variance of said first set of critical dimension error measurements (VCD_A), mean error of said first set of critical dimension error measurements (dCD_A), variance of said second set of critical dimension error measurements (VCD_B), mean error of said second set of critical dimension error measurements (dCD_B), and said line edge placement specification (SPEC).

5. The method of Claim 4 wherein said overlay tolerance for said lot of semiconductor wafers is determined according to the following equation:

$$OT = \sqrt{(SPEC - dCD_A - dCD_B)^2 - \left(\frac{VCD_A}{2}\right)^2 - \left(\frac{VCD_B}{2}\right)^2}.$$

6. The method of Claim 1 wherein said overlay tolerance for said lot of semiconductor wafers is determined using a graph.

7. A method for determining whether a lot of semiconductor wafers should be reworked comprising:

measuring a first patterned layer on some of said semiconductor wafers so as to obtain a first set of critical dimension error measurements;

measuring a second patterned layer on some of said semiconductor wafers so as to obtain a second set of critical dimension error measurements;

measuring overlay error between said first patterned layer and said second patterned layer on some of said semiconductor wafers; and

reworking said lot of semiconductor wafers when said measured overlay error exceeds an overlay tolerance determined using said first set of critical dimension error measurements, said second set of critical dimension error measurements, and said line edge placement specification.

8. The method of Claim 7 wherein said overlay tolerance is determined using variance of said first set of critical dimension error measurements (VCD_A), mean of said first set of critical dimension error measurements (dCD_A), variance of said second set of critical dimension error measurements (VCD_B), mean of said

second set of critical dimension error measurements (dCD_B), and said line edge placement specification (SPEC).

9. The method of Claim 8 wherein said overlay tolerance is determined according to the following equation:

$$OT = \sqrt{(SPEC - dCD_A - dCD_B)^2 - \left(\frac{VCD_A}{2}\right)^2 - \left(\frac{VCD_B}{2}\right)^2}.$$

10. A computer-implemented method for determining overlay tolerance comprising:

receiving a first set of critical dimension error measurements, said first set of critical dimension error measurements indicating critical dimension error of a first patterned layer formed on a plurality of semiconductor wafers;

receiving a second set of critical dimension error measurements, said second set of critical dimension error measurements indicating critical dimension error of a second patterned layer formed on said semiconductor wafers;

receiving a line edge placement specification for said semiconductor wafers; and

calculating overlay tolerance using said first set of critical dimension error measurements, said second set of critical dimension error measurements, and a line edge placement specification for said semiconductor wafers.

11. The computer-implemented method of Claim 10 wherein said calculating overlay tolerance further comprises:

calculating overlay tolerance (OT) using variance of said first set of critical dimension error measurements (VCD_A), mean of said first set of critical dimension error measurements (dCD_A), variance of said second set of critical dimension error measurements (VCD_B), mean of said second set of critical dimension error measurements (dCD_B), and said line edge placement specification (SPEC).

12. The computer-implemented method of Claim 11 wherein said overlay tolerance is determined according to the following equation:

$$OT = \sqrt{(SPEC - dCD_A - dCD_B)^2 - \left(\frac{VCD_A}{2}\right)^2 - \left(\frac{VCD_B}{2}\right)^2}.$$

13. A method for determining critical dimension tolerance for a lot of semiconductor wafers comprising:

measuring overlay error between a first patterned layer and a second patterned layer on some of said semiconductor wafers so as to obtain a first set of overlay error measurements; and

determining critical dimension tolerance for said lot of semiconductor wafers using said overlay error measurements and using a line edge placement specification for said semiconductor wafers.

14. The method of Claim 13 wherein said critical dimension tolerance is determined using mean error of said overlay error measurements (dO_{B-A}), variance of said overlay error measurements (VO_{B-A}) and said line edge placement specification (SPEC).

15. The method of Claim 14 wherein said critical dimension tolerance (CDT) is determined according to the following equation:

$$CDT = \sqrt{(SPEC - dO_{B-A})^2 - \left(\frac{VO_{B-A}}{2}\right)^2}.$$

16. A method for determining whether a lot of semiconductor wafers should be reworked comprising:

measuring overlay error between a first patterned layer and a second patterned layer on some of said semiconductor wafers so as to obtain a plurality of overlay error measurements;

measuring critical dimension error of said second patterned layer on some of said semiconductor wafers; and

reworking said lot of semiconductor wafers when said measured critical dimension error exceeds a critical dimension tolerance determined using said overlay error measurements and a line edge placement specification.

17. The method of Claim 16 wherein said critical dimension tolerance is determined using variance of said overlay error measurements (VO_{B-A}), mean of said overlay error measurements (dO_{B-A}) and said line edge placement specification (SPEC).

18. The method of Claim 17 wherein said critical dimension tolerance (CDT) is determined according to the following equation:

$$CDT = \sqrt{(SPEC - dO_{B-A})^2 - \left(\frac{VO_{B-A}}{2}\right)^2}.$$

19. A computer-implemented method for determining critical dimension tolerance for a lot of semiconductor wafers comprising:

receiving a plurality of overlay error measurements, said overlay error measurements indicating overlay error between a first patterned layer and a second patterned layer on some of said semiconductor wafers;

receiving a line edge placement specification for said semiconductor wafers; and

calculating critical dimension tolerance for said lot of semiconductor wafers using said overlay error measurements and using said line edge placement specification.

20. The computer-implemented method of Claim 19 wherein said critical dimension tolerance (CDT) is calculated using variance

of said overlay error measurements (VO_{B-A}), mean of said overlay error measurements (dO_{B-A}) and said line edge placement specification (SPEC).

21. The computer-implemented method of Claim 20 wherein said critical dimension tolerance is calculated according to the following equation:

$$CDT = \sqrt{(SPEC - dO_{B-A})^2 - \left(\frac{VO_{B-A}}{2}\right)^2}.$$

22. A method for determining an estimate of line edge placement error for a lot of semiconductor wafers comprising:

measuring a first patterned layer on some of said semiconductor wafers so as to obtain a first set of critical dimension error measurements;

measuring a second patterned layer on some of said semiconductor wafers so as to obtain a second set of critical dimension error measurements;

measuring some of said semiconductor wafers so as to obtain a set of overlay error measurements; and

determining an estimate of line edge placement error for said lot of semiconductor wafers using said first set of critical dimension error measurements, said second set of critical dimension error measurements, and said set of overlay error measurements.

23. The method of Claim 22 wherein said determining an estimate of line edge placement error further comprises:

determining an estimate of line edge placement error using variance of said first set of critical dimension error measurements (VCD_A), mean of said first set of critical dimension error measurements (dCD_A), variance of said second set of critical dimension error measurements (VCD_B), mean of said second set of critical dimension error measurements (dCD_B), variance of said set of overlay error measurements (VO), and mean of said set of overlay error measurements (dO).

24. The method of Claim 23 wherein said estimate of line edge placement error is a mean $+3\sigma$ estimate.

25. The method of Claim 24 wherein said estimate of line edge placement error (D) is determined according to the following equation:

$$D = dO + \left(\frac{dCD_A}{2}\right) + \left(\frac{dCD_B}{2}\right) + \sqrt{\left(\frac{VCD_A}{2}\right)^2 + \left(\frac{VCD_B}{2}\right)^2 + VO^2}\ .$$

26. The method of Claim 25 wherein said estimate of line edge placement error is a single number that indicates the error state of said lot of semiconductor wafers.

27. A method for determining whether a lot of semiconductor wafers should be reworked comprising:

measuring a first patterned layer on some of said semiconductor wafers so as to obtain a first set of critical dimension error measurements;

measuring a second patterned layer on some of said semiconductor wafers so as to obtain a second set of critical dimension error measurements;

measuring some of said semiconductor wafers so as to obtain a set of overlay error measurements that indicate the overlay error between said first patterned layer and said second patterned layer;

determining an estimate of line edge placement error for said lot of semiconductor wafers using said first set of critical dimension error measurements, said second set of critical dimension error measurements, and said set of overlay error measurements; and

reworking said lot of semiconductor wafers when said estimate of line edge placement error exceeds a line edge placement specification.

28. The method of Claim 27 wherein said estimate of line edge placement error is determined using variance of said first set of critical dimension error measurements (VCD_A), mean of said first

set of critical dimension error measurements (dCD_A), variance of said second set of critical dimension error measurements (VCD_B), mean of said second set of critical dimension error measurements (dCD_B), variance of said set of overlay error measurements (VO), and mean of said set of overlay error measurements (dO).

29. The method of Claim 28 wherein said estimate of line edge placement error is a mean $+3\sigma$ estimate and wherein said line edge placement specification is a mean $+3\sigma$ specification.

30. The method of Claim 29 wherein said estimate of line edge placement error (D) is determined according to the following equation:

$$D = dO + \left(\frac{dCD_A}{2}\right) + \left(\frac{dCD_B}{2}\right) + \sqrt{\left(\frac{VCD_A}{2}\right)^2 + \left(\frac{VCD_B}{2}\right)^2 + VO^2}\ .$$

31. A computer-implemented method for determining whether a lot of semiconductor wafers needs to be reworked comprising:

receiving a first set of critical dimension error measurements, said first set of critical dimension error measurements indicating critical dimension error of a first patterned layer for some of said semiconductor wafers;

receiving a second set of critical dimension error measurements, said second set of critical dimension error

measurements indicating critical dimension error of a second patterned layer for some of said semiconductor wafers;

receiving a set of overlay error measurements, said set of overlay error measurements indicating overlay error between said first patterned layer and said second patterned layer on some of said semiconductor wafers; and

calculating an estimate of line edge placement error using said first set of critical dimension error measurements, said second set of critical dimension error measurements, and said set of overlay error measurements.

32. The computer-implemented method of Claim 31 further comprising:

receiving a line edge placement specification for said semiconductor wafers; and

indicating that said semiconductors should be reworked when said estimate of line edge placement error exceeds said line edge placement specification.